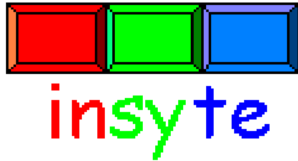
Credence Toolbox
Application Note BD-04



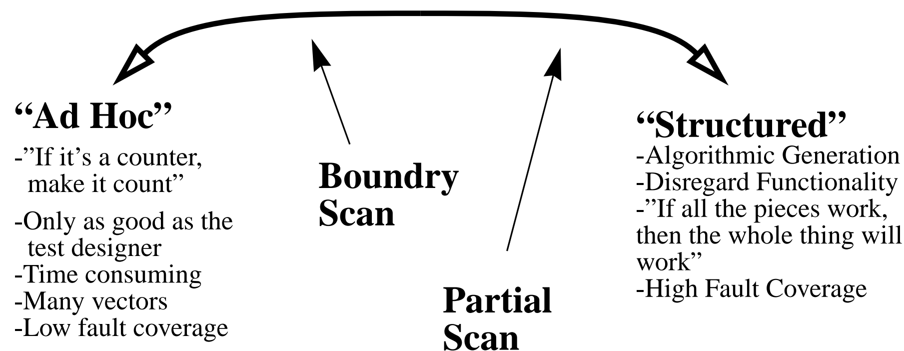
SCAN TEST OVERVIEW

Contributed by: Peter Lindholm

July 24, 1999

This Application Note contains a brief overview of Scan test logic elements,design considerations, test considerations and general implementation on VistaLogic/Logic100 series testers. For further information on test program implementation, please see Credence Application Notes 8 and 67.

The "Test Continuum"



Scan Design Considerations

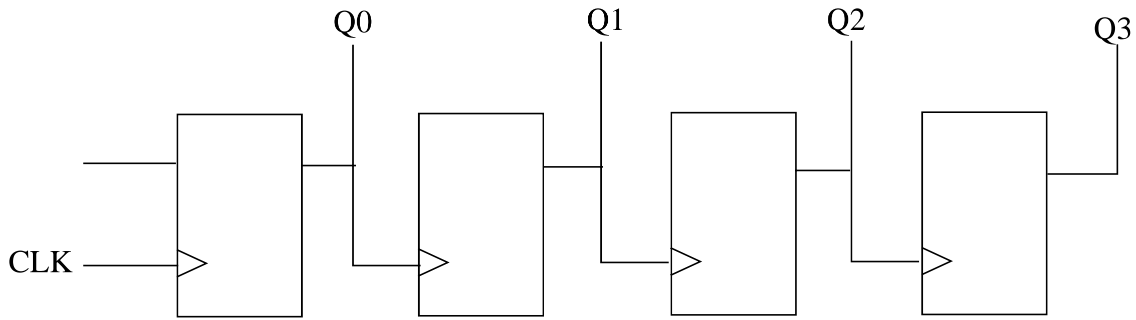
+10 % die size

+10 % prop delay (Capacitance)

Special design/DFT software tools required

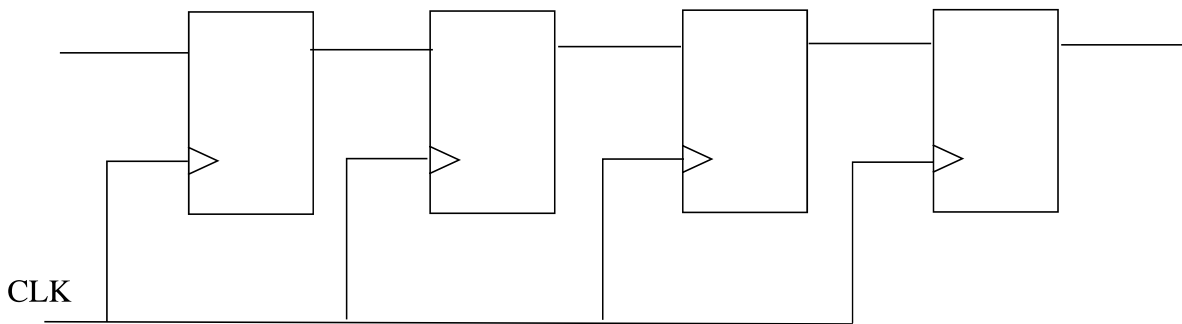
Scan logic element library required

Scan Test Considerations



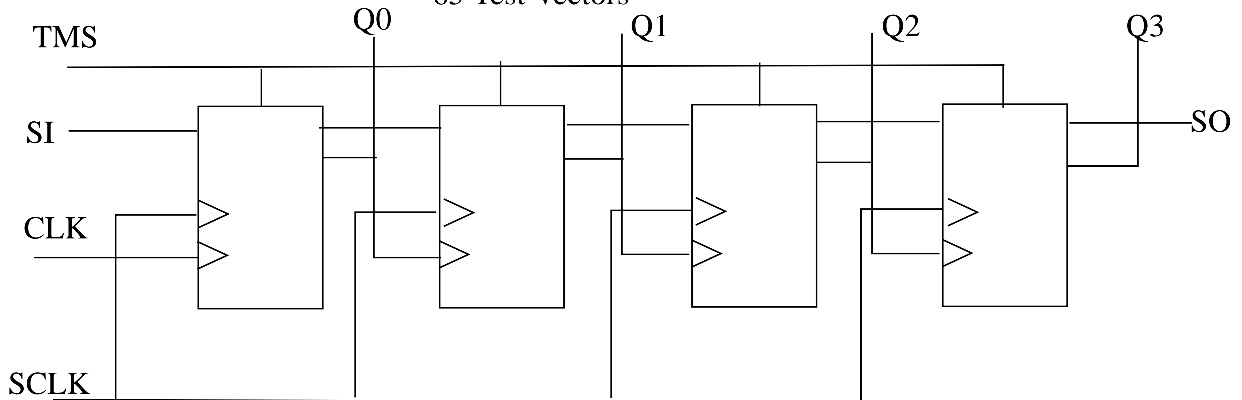
4-Bit Counter
Test Vectors = 17 (2^n + 1)

64-Bit Counter -> ???



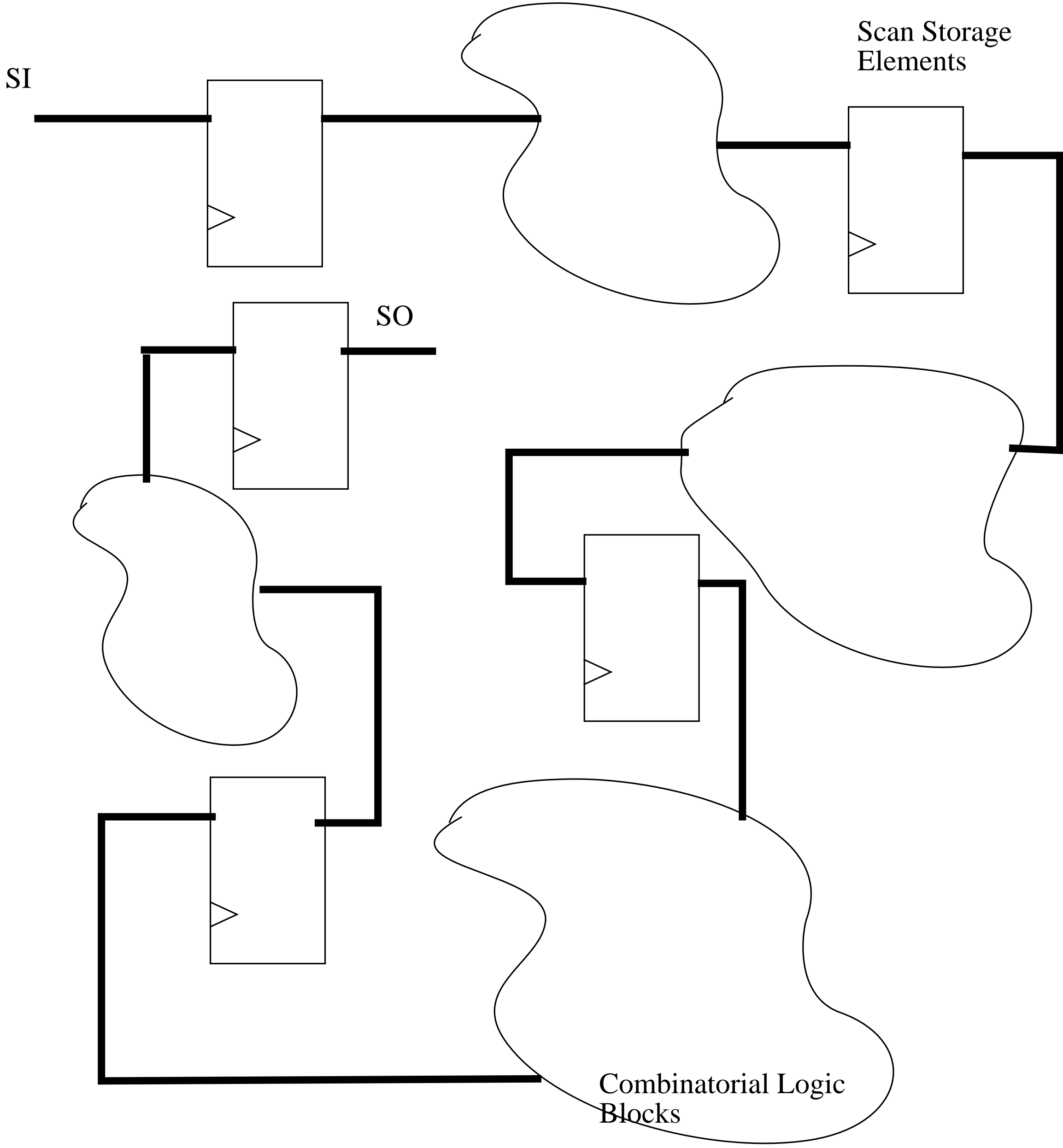
4-Bit Shift Register
Test Vectors = 5 (n + 1)

64-Bit Shift Register
65 Test Vectors



Combine Both Elements
Add a Control Pin (Test Mode Select)
Circuit Can be Used Both Ways

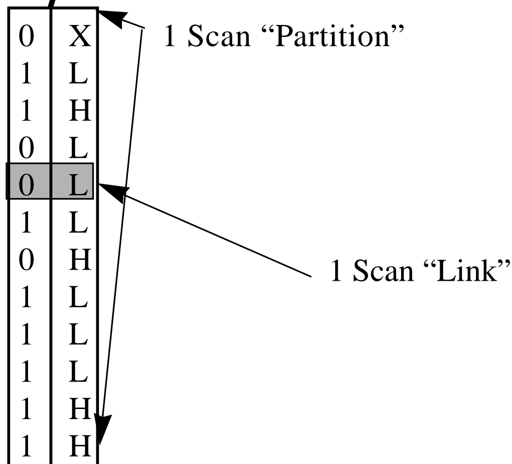
Scan Elements in a Circuit Design



Test Method and Implementation:

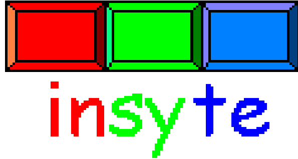
- Use Scan to Preload Storage Elements (Scan F-Fs) to Known State
- Use Normal Vectors to Clock Data into a Combinatorial Block from Scan F-F
- New Data is Clocked into Storage Elements from each Combinatorial Block into the Subsequent Scan F-F
- Use Scan to Unload Data from Scan F-Fs

IN1	SI	SO	OUT1	SCLK	CLK	TMS	
0	0	X	L	0	1	0	"Flat" or Parallel Vector
1	0	X	L	0	1	0	
1	0	X	X	1	0	1	CLK->off; SCLK->on; TMS->on for Scan Vector Parallel Vector Repeated During Scan for n=12 times
0	0	X	H	0	1	0	Parallel Vector to Clock Data Through Combinatorial Logic
1	0	L	X	1	0	1	Next Scan Vector



For further information, contact:
Integrated Systems Test
1572 Massachusetts Avenue
Cambridge, MA 02138
(617) 876-7756
www.insyte-ate.com

Credence Toolbox
Application Note BD-04



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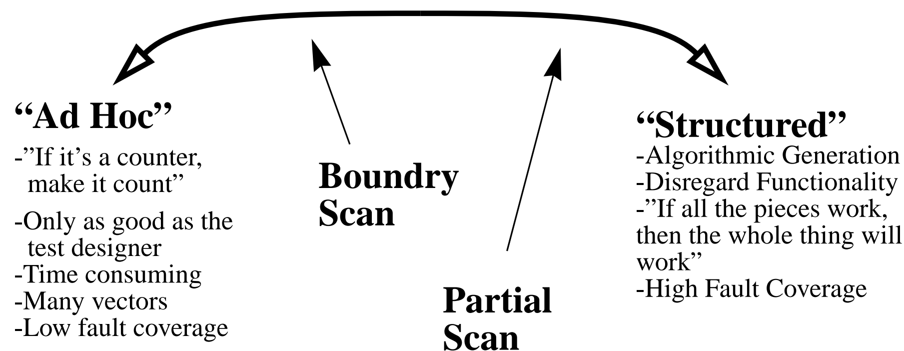

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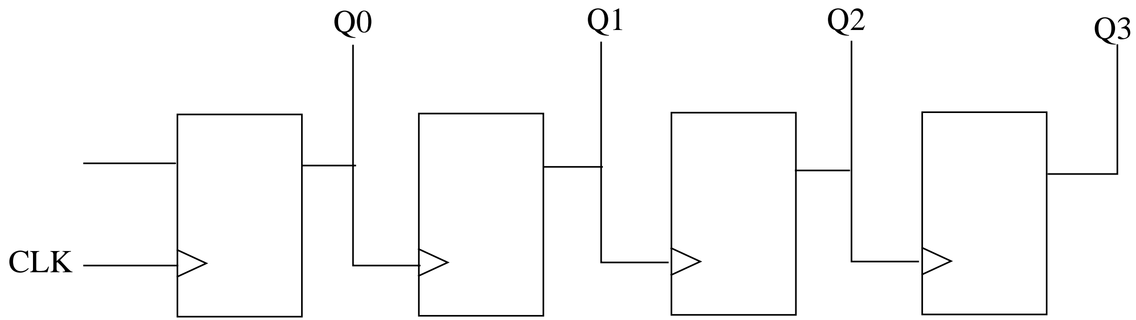

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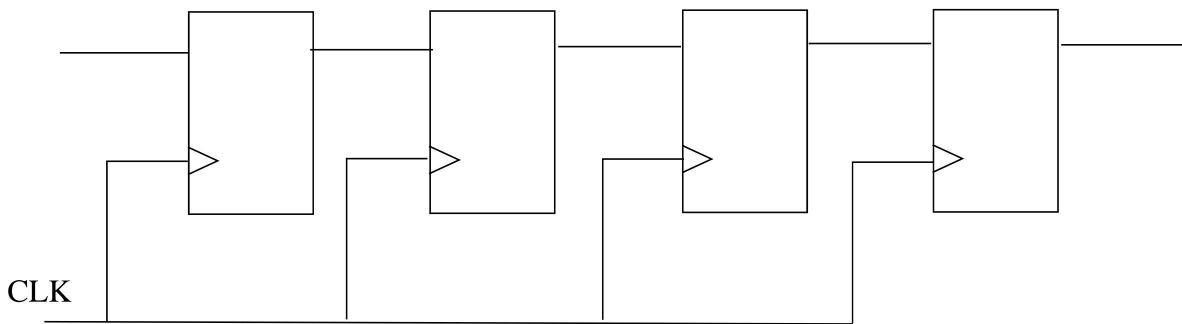

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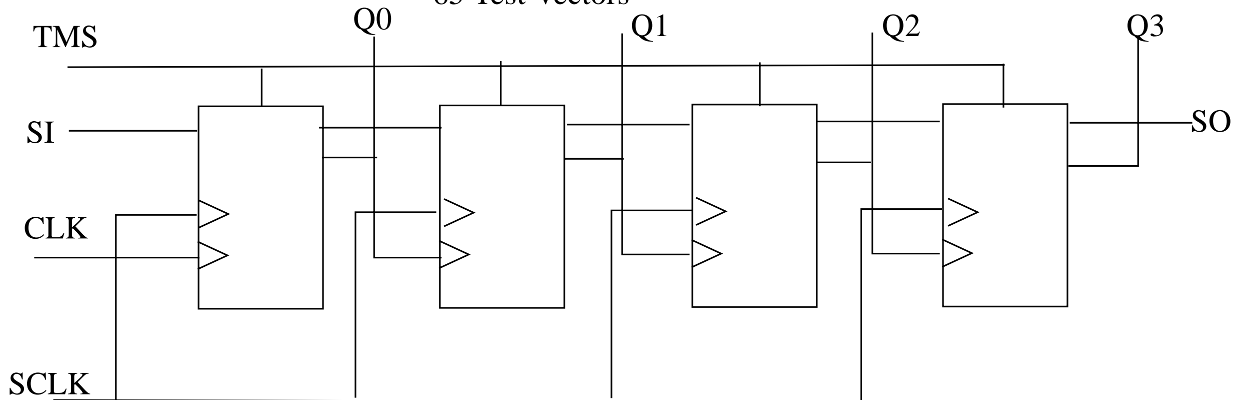

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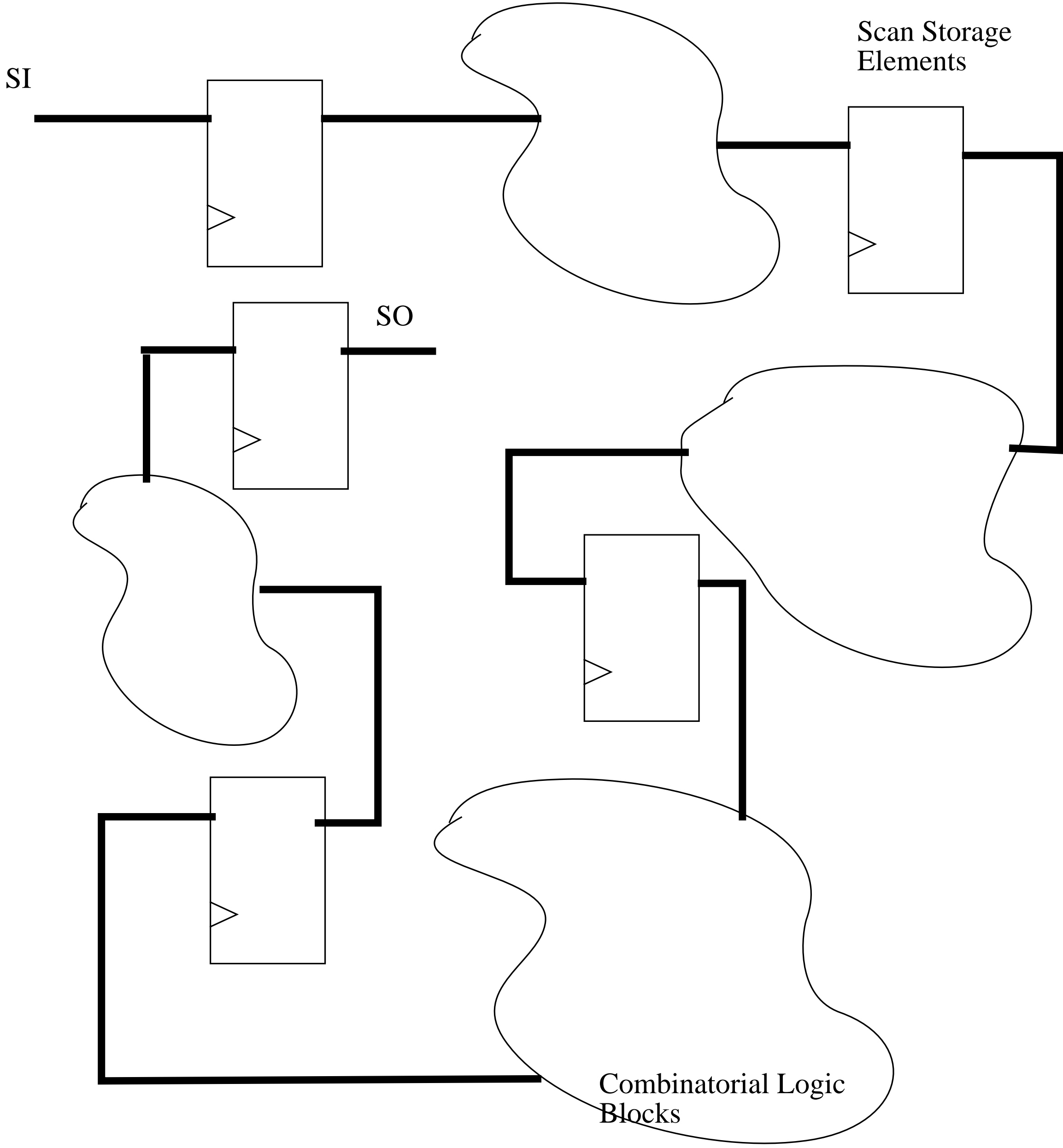
Scan Elements in a Circuit Design



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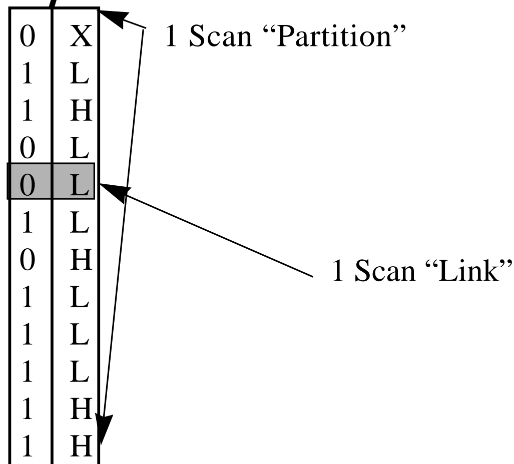

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